1. General Description

G1610 is a highly integrated Green Mode PWM control IC, It minimizes the component counts,circuit space,and reduces the overall material cost for the power applications.

The G1610 features green-mode power-saving operation,auto gain control,and internal slope compensation,soft-start functions to optimized high performance,low standby power consumption and wide output voltage range PD adapter solutions.

At full loading,the IC operates in fixed fequency mode.When the loading goes low,it operates in Green mode with valley switching for high power conversion efficiency. When the load is very small, the IC operates in Extended Burst Mode to minimize the standby power loss. As a result,high conversion efficiency can be achieved in the whole loading range.

G1610 offers complete protection coverage including cycle-by-cycle current limiting(OCP), over temperature protection(OTP), output short, output and VDD over voltage protection.Excellent EMI performance is achieved with proprietary frequency shuffling technique.

Applications

Offline AC/DC flyback converter for

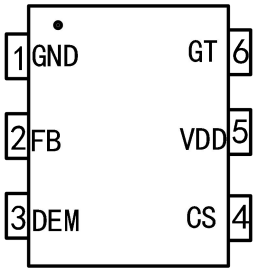
- PD adapters
- Wide output range adapters
- Open Frame Switching Power Supply

Features

- Ultra low operating current at light/no load
- Adaptive loop gain compensation
- Extended burst mode control for improved efficiency and low standby power
- Frequency Conversion Mode Operation with 65KHz or 45KHz fixed frequency@ FullLoad
- Peak Load Mode with 125KHz max frequency
- Valley switching operation @Green mode
- Internal OCP compensation for universal line voltage
- Power on soft start reducing MOSEFT Vds stress
- Audio noise free operation
- Protection Features
  - •VDD UV lockout and Over voltage protection
  - •Cycle-by-Cycle over current protection with auto-recovery
  - •Output over voltage protection with latch shut down
  - •Secondary rectifier diode open and short circuit protection with auto-recovery
  - •Secondary winding Open and short circuit protection with auto-recovery
  - •Output short protection(SCP) with auto-recovery
  - •Over temperature protection(OTP) with latch shut down
  - •Overload protection (OLP) with auto-recovery
- Pb-free SOT23-6

2. Products Information

2.1 Pin configuration



SOT23-6 Package

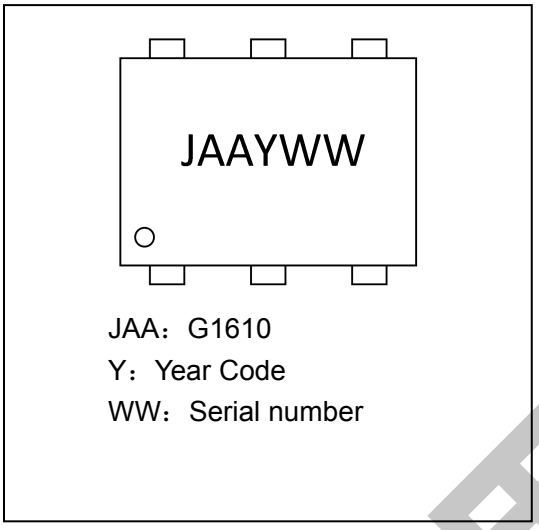
Fig.1. G1610 Pin Configuration

Pin Name	I/O	Description
GND	P	Ground.
FB	I	Feedback input pin.By connecting an opto-coupler to close the control loop and achieve the regulation.
DEM	I	Multiple functions pin.Connecting a NTC resistor to ground for OTP detection.Connecting a resistor from Vaux can adjust IOVP/ISCP trigger current and detect transformer core demagnetization.If both OTP and OVP/SCP are needed,a diode should be connected between DEM pin and the NTC resistor.
CS	I	Current sense input,connect it to sense the MOSFET current.
VDD	P	Power Supply.
GT	O	Gate driver output to driver the external MOSFET.

2.2 Ordering Information

Part Number	Marking ID	Package	Packing
G1610	JAAXXX	SOT23-6	3000/Tape&Reel

2.3 Marking Information



Year Code

A	B	C	D	E	F	G	H	I	J	K	L	M
2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
N	O	P	Q	R	S	T	U	V	W	X	Y	Z
2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038

2.4 Block diagram

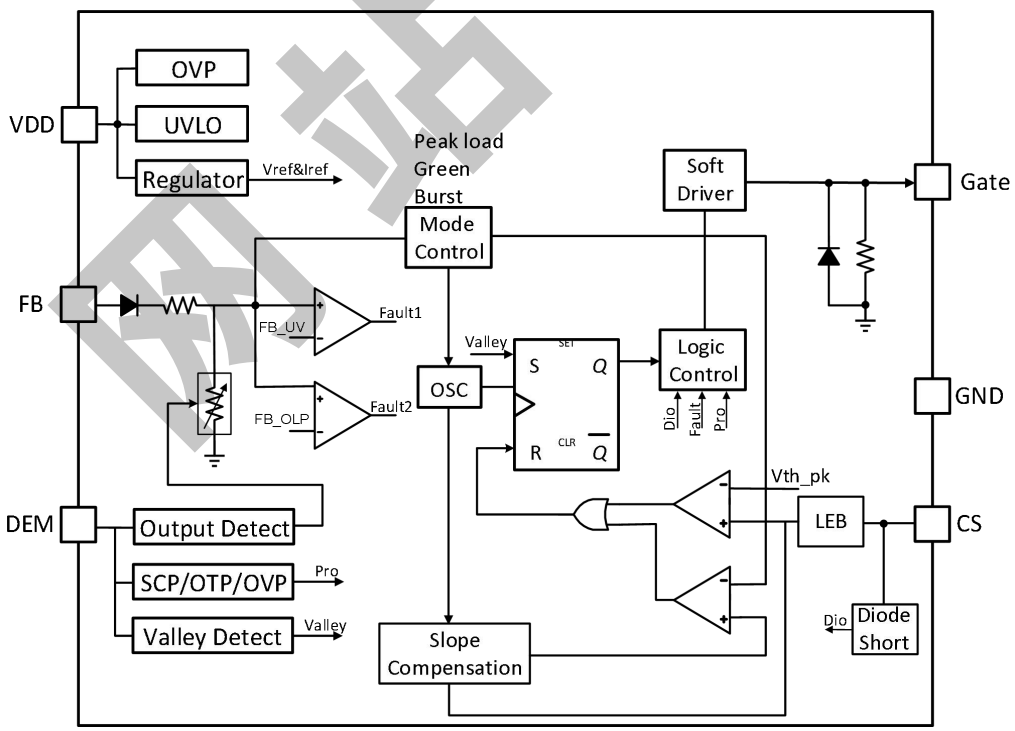


Fig.2. Block Diagram

3. Absolute Maximum Ratings

Description	Absolute Maximum Ratings
VDD Voltage	85V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
DEM Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150℃
Operating Ambient Temperature T_A	-40 to 85℃
Min/Max Storage Temperature T_{stg}	-55 to 150℃
Lead Temperature (Soldering, 10secs)	260℃
Package Dissipation Rating for SOT23-6 $R_{\theta JA}$	200℃/W

Notes:

Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

4. Electrical Characteristics

(TA = 25℃, VDD=18V, unless otherwise noted)

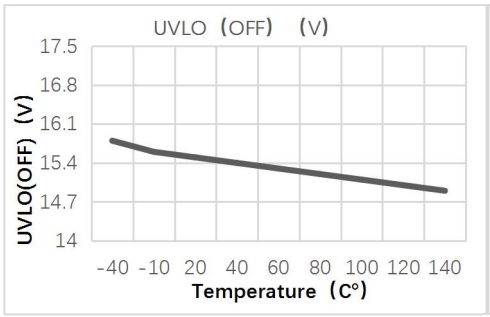
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage（VDD）						
I_{VDD_ST}	VDD start up current	VDD=U_{VLO_OFF}-1V,measure leakage current into VDD		5	20	uA
I_{VDD_OP}	Normal operation Current	V_{FB}=3V,CL=1nF		2	2.5	mA
$I_{VDD\_OP\_Burst}$	Burst operation Current	V_{FB}=0.5V,CL=1nF		0.4	0.45	mA
U_{VLO_ON}	VDD Under Voltage Lockout Enter	VDD falling	6	7	8	V
U_{VLO_OFF}	VDD Under Voltage Lockout Exit	VDD rising	14.5	15.5	16.5	V
$V_{pull-up}$	Pull-up PMOS active			10		V
V_{DD_OVP}	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	82	84	86	V
V_{th_latch}	Latch release Voltage			4.8		V
$T_{D\_recovery}$	Restart time for auto-recovery protection			1.4		S
Feedack Input Section（FB Pin）						
V_{FB_OPEN}	V_{FB} open loop voltage			5.1		V
A_{VCS}	PWM input gain △V_{FB}/△V_{CS}	I_{OVP}≥170uA with hysteresis		2.8		V/V
		95≤I_{OVP}≤150uA with hysteresis		3.5		V/V
		I_{OVP}≤85uA with hysteresis		4.5		V/V
D_{MAX}	Max duty cycle @VDD=14V,V_{FB}=3V,V_{CS}=0.3V	I_{OVP}＞95uA		80		%
V_{ref_rising}	The threshold enter rising frequency mode	I_{OVP}＞243uA		3.5		V
V_{ref_green}	The threshold enter green mode			1.8		V
$V_{ref\_burst\_H}$	The threshold exit burst mode			1.2		V
$V_{ref\_burst\_L}$	The threshold enter burst mode			1.1		V
I_{FB_short}	FB pin short circuit current	Short FB pin to GND and measure current		200		uA

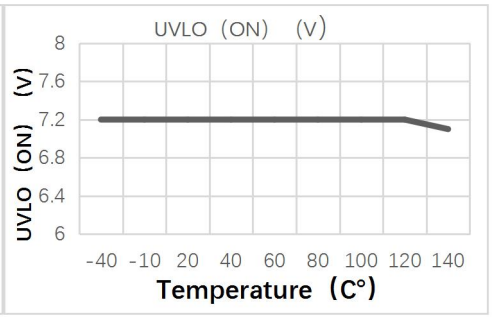
$V_{TH\_openloop}$	The open loop FB threshold voltage			4.5		V
$T_{D\_openloop}$	The open loop protection debounce time			40		ms
Z_{FB_IN}	Input impedance			30		KΩ
Current Sense Input（CS Pin）						
SST	Soft start time of CS threshold			4		ms
T_{LEB}	Leading edge blanking time			300		ns
T_{D_OC}	Over current detection and control delay	From over current occurs till the gate driver output starts to turn off		90		ns
V_{ref_PK}	Internal current limiting threshold voltage with zero duty cycle		0.48	0.50	0.52	V
$V_{ref\_PK\_clamp}$	CS voltage clamper			0.85		V
$T_{d\_CS\_PK\_ADJ}$	The delay time from PWM off to CS peak clamping adjustment start point			2.5		us
I_{OCP_ADJ}	Output current from CS pin when PWM turns off		92	100	108	uA
T_{D_OCP}	OCP debounce time			60		ms
Oscillator						
F_{osc_nom}	Normal Fixed Oscillation Frequency of high output voltage	VDD=15V,FB=3V,I_{OVP}＞95uA	60	65	70	KHZ
F_{osc_low}	Normal Fixed Oscillation Frequency of low output voltage	I_{OVP}＜85uA		45		KHZ
F_{osc_PK}	Peak frequency	VDD=15V,FB=4.5V,I_{OVP}＞245uA		125		KHZ
$\triangle f_{\_osc}$	Frequency jittering			±7		%
$F_{\_shuffling}$	Shuffling frequency			240		HZ
$\triangle f_{\_Temp}$	Frequency temperature stability			1		%
$\triangle f_{\_VDD}$	Frequency voltage stability			1		%
$F_{\_Burst}$	Burst mode switch frequency			23		KHZ
Gate Driver（GT Pin）						
V_{OL}	Output low level	VDD=15V,I_O=20mA			1	V

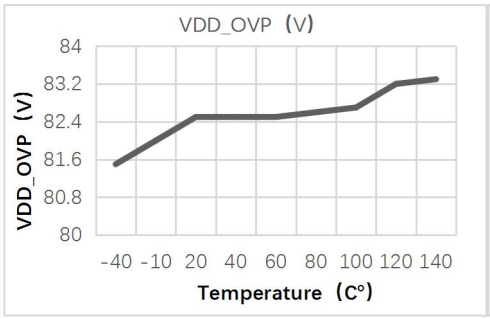
V_{OH}	Output high level	VDD=15V,I_O=20mA	8			V
V_{CLAMP}	Output clamp voltage			12		V
T_r	Output rising time 1.2V~10.8V	CL=1000pF		140		ns
T_f	Output falling time 10.8V~1.2VCL=1000pF	CL=1000pF		55		ns
DEM Pin						
I_{bias}	Output bias current expect during OVP detection			30		uA
I_{DEM}	Output current for external OTP detection		114	120	126	uA
V_{OTP}	Threshold voltage for external OTP		1.14	1.2	1.26	V
$T_{d\_ex\_OTP}$	EX OTP debounce time			60		cycles
I_{output_OVP}	Current threshold for adjustable output OVP		340	360	380	uA
$T_{d\_output\_OVP}$	Output OVP debounce time			8		cycles
T_{samp_OVP}	The time from Gate off to OVP detecting turn-off point	FB=2.5V		2.5		us
		FB=1.5V		1.8		us
I_{scp}	SCP threshold	T＜15ms after startup		23		uA
T_{d_scp}	SCP debounce time			8		cycles
On chip OTP						
T_{SD}	OTP shutdown Threshold			155		℃
T_{SD_R}	OTP shutdown recovery			125		℃

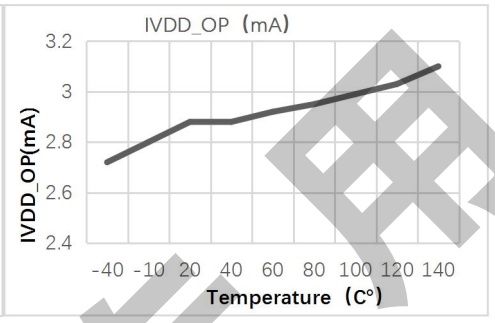
Note:These parameters are not 100% tested, guaranteed by design and characterization.

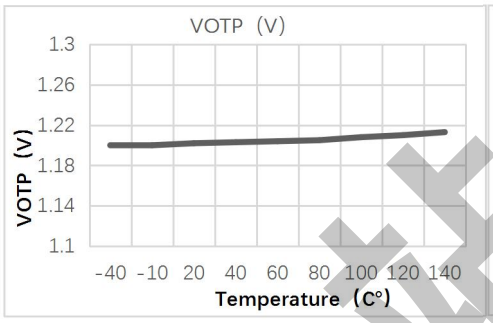
5. CHARACTERIZATION

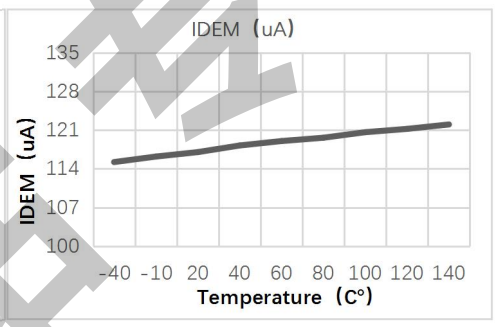


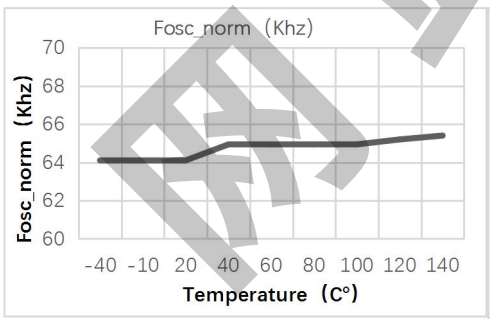


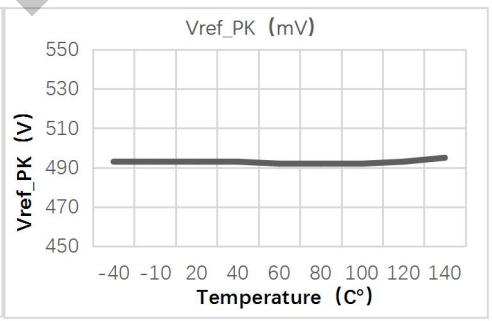












6. OPERATION DESCRIPTION

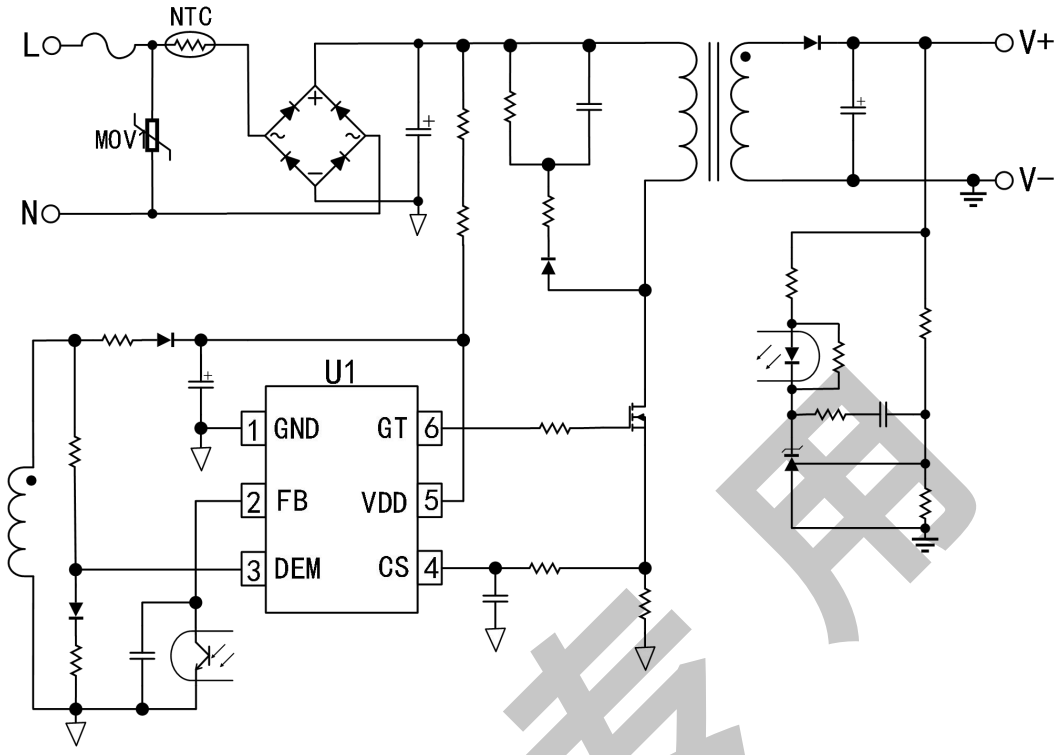


Fig.3. G1610 Typical Application

G1610 is a highly integrated current mode PWM control IC,included high performance,low standby power consumption and wide output voltage range PD secondary controller.

6.1 Startup Current and Startup Control

The startup current of G1610 is designed to be very low so that VDD could be charged up above UVLO (off) threshold level and device starts up quickly. Also a large value startup resistor can be used to minimize the power loss.The operating current of G1610 is as low as 2mA. Good efficiency is achieved with the low operating current together with Extended burst mode control features.

6.2 Soft Start

To prevent audible noise and soften the electrical stress during start-up or a restart condition, an integrated soft start feature is implemented. As soon as VDD reaches UVLO(OFF), the CS peak voltage is gradually increased from 0V to the maximum level.Every restart up is followed by a soft start. The soft start time constant is 4 ms, set by an internal time.

6.4 Internal Slope Compensation and Adaptive Loop Gain Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%.To stabilize the control loop,the slope compensation is required in the traditional IC design by injecting the ramp signal from the additional pin through a coupling capacitor.G1610 has internal slope compensation circuit to simplify the external circuit design.

With proprietary technology,an adaptive loop compensation is implemented to ensure the system loop stability for wide output voltage range according to lovp current detection.

6.5 Frequency Jitter

The G1610 is build in with frequency jitter function, which makes it easy for the power supply designers to optimize EMI performance and system cost.The frequency jitter is internally set for ±7%.

6.6 Extended Burst Mode Operation

At light load or no load condition, the switch loss become the major loss of the power supply, to reduce the power wasted in such conditions, based on a special designed voltage controlled oscillator, green mode operation of the power supply can be achieved by using G1610.

The switching frequency is internally adjusted at no load or light load condition.The switch frequency reduces at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below $V_{ref\_burst\_L}$(the threshold enter burst mode) and device enters Burst Mode control.The gate drive output switches when FB input rises back to $V_{ref\_burst\_H}$(the threshold exit burst mode).Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.The switching frequency control also eliminates the audio noise at any loading conditions.

6.7 Oscillator Operation

During the full load power operation,G1610 operates at a fixed frequency(65KHz) of high output voltage, and it operates at a fixed frequency(45KHz) of low output voltage. The efficiency and system cost is controlled at an optimal level. A peak power mode is implemented to supply a peak current output requirement. In peak power mode,frequency is increased from 65KHz to 125KHz.

At light load,G1610 enters the light load mode,where the output current is reduced.The switching lossers are reduced by lowering the switching frequency.

6.8 Current Sensing and LEB

Cycle-by-Cycle current limiting is offered in G1610. The switch current is detected by a sense resistor into the CS pin.An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET.The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period.The PWM duty cycle is determined by the current sense voltage and the FB voltage.

6.9 Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through DEM pin.This voltage features a flyback polarity. Demagnetization is recognized by detection of a possible “valley” when the voltage at DEM is below 85mV in falling edge.

6.10 external OTP and output OVP/SCP

proprietary dual function of external OTP and output OVP provides feasible and accurate detection of external OTP through NTC resistor and output OVP.The dual function is realized through time-division technology.

6.11 Programmable OCP and Peak Output Current Control

In order to meet peak current output requirement,G1610 sets up two levels output current protection thresholds.The two thresholds correspond to the normal OCP protection and peak power protection respectively.When output current exceeds the OCP threshold for 60ms(typical),OCP protection occurs.The OCP loop ensures the output OCP has a very tight range and is only related with turns ratio and Rsense. With proprietary technology,the OCP is line voltage compensated to achieve constant output OCP limit over the universal input voltage range and its dependency on primary inductance and frequency is removed.

6.12 Two level OCP controls

In order to meet peak current output requirement under high output level,G1610 sets up two levels OCP protection thresholds.The two thresholds correspond to the normal OCP protection and peak power protection respectively,and these two threshold values are internally compensated. When primary side inductor current exceeds the OCP threshold,OCP timer will begin counting.After 60ms(typical),OCP protection occurs.

When primary side inductor current exceeds the peak power threshold,over peak power timer will begin counting.After 40ms(typical),peak load protection occurs.OCP and peak power protection are mutually independent and do not affect each.

When OCP or peak power protection occurs, no GATE output and VDD begins discharging and charging until the duration is longer than 1.4s.Then VDD begins to drop until to UVLO(on) and later restarts.

6.13 Driver

The output stage of G1610 is a fast totem pole gate driver. Dead time has been added to minimize heat dissipation, increases efficiency and enhances reliability. The output driver is clamped by an internal 11.5V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage. A soft driving waveform is implemented to minimize EMI.

6.14 Pin floating and short protection

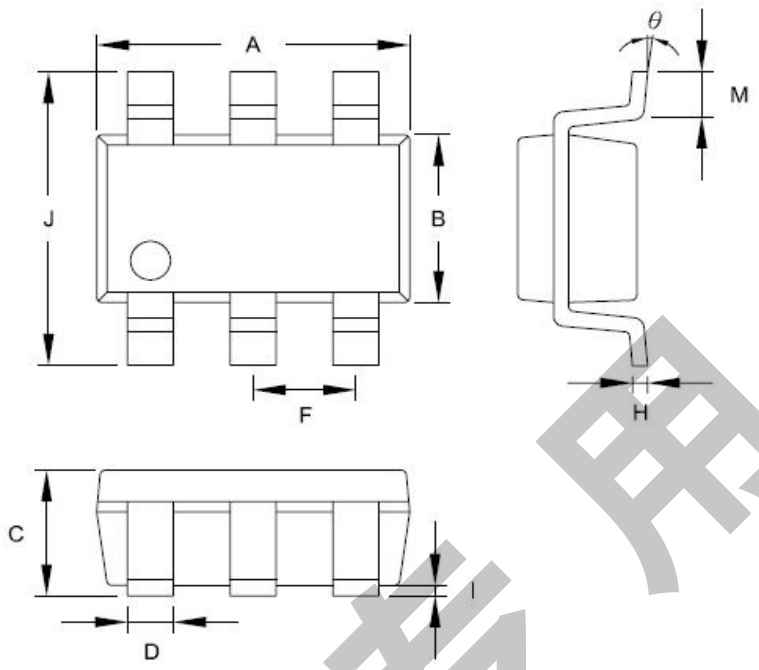
G1610 provides pin floating protection for all the pins and pin short protection for adjacent pins.In the cases when a pin is floating or two adjacent pins are shorted,Gate switching is disabled.

6.15 Protection controls

To increase the reliability of power supply system,many protection functions are integrated in this controller,including Cycle-by-Cycle current limiting (OCP),VDD over Voltage Protection,Output over voltage protection (OVP),over temperature protection (OTP),Over load Protection (OLP),output diode short protection.At overload condition when FB input voltage exceeds power limit threshold value for more than $T_{D\_openloop}$(The open loop protection debounce time),the controller reacts to shut down the output power MOSFET.Device restarts when VDD voltage drops below UVLO limit. VDD is supplied by transformer auxiliary winding output.OVP is triggered when VDD is higher than threshold value.The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

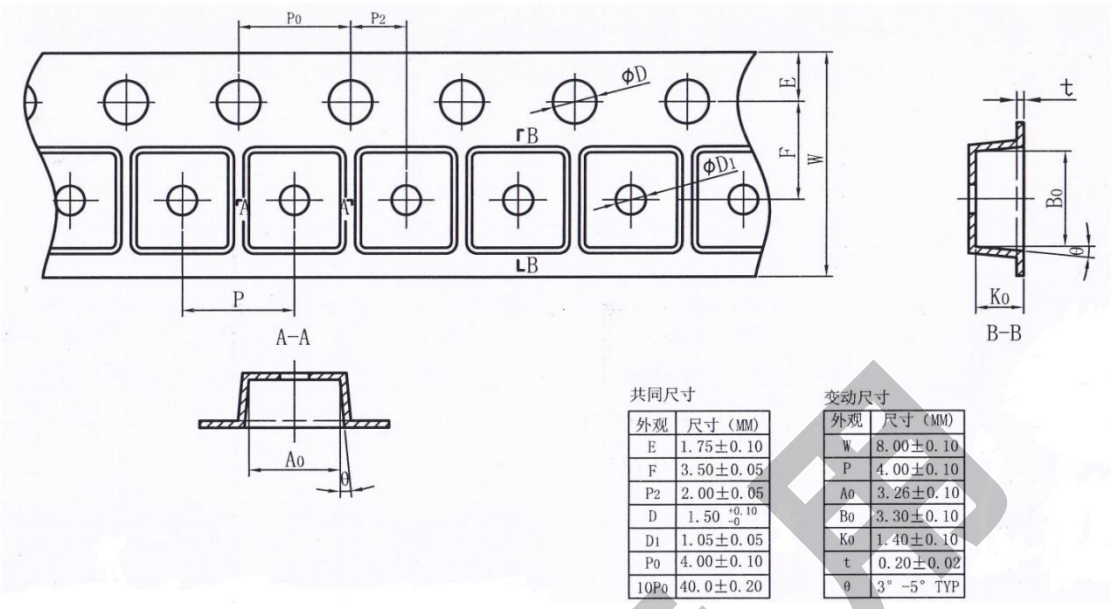
7. Package Information

SOT23-6:



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	--	1.450	--	0.057
D	0.300	0.500	0.012	0.020
F	0.95	--	0.037	--
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

8. Tape and Reel Information

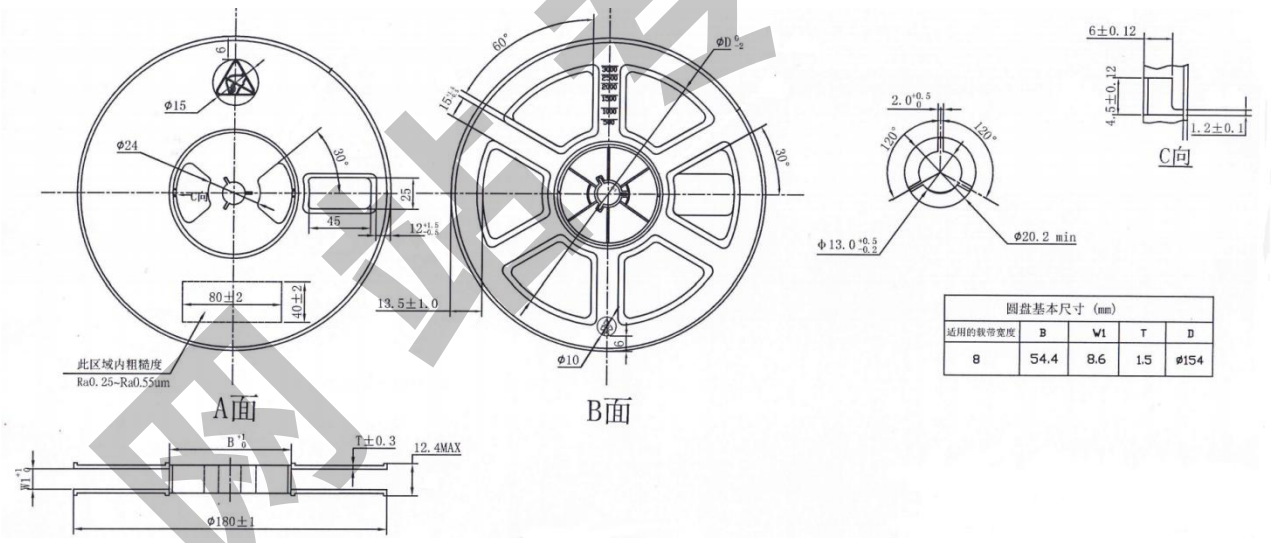


共同尺寸

外观	尺寸 (MM)
E	1.75±0.10
F	3.50±0.05
P2	2.00±0.05
D	1.50 +0.10 −0
D1	1.05±0.05
P0	4.00±0.10
10P0	40.0±0.20

变动尺寸

外观	尺寸 (MM)
W	8.00±0.10
P	4.00±0.10
A0	3.26±0.10
B0	3.30±0.10
K0	1.40±0.10
t	0.20±0.02
θ	3° -5° TYP



Addendum：

IR-Reflow Profile For Pb-fre Leads

Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See Pb-free Process
Time within 5°C of actual Peak Temperature (tp)	20-40 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Notes: All temperatures refer to topside of the package. Measured on the body surface.